  
**Course:** EE200 Digital Logic Design

**Course Instructor:** Muhammad Abbas Khan

Semester: Spring-2024

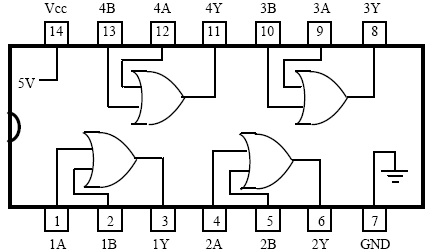
Department of Computing

**Lab Task no.** **3: Verification of Truth Table of OR Logic Gates**

**APPARATUS:**

OR (7432), Digital Logic Trainer, Connecting wires.

**OR Gate (7432)**



**TRUTH TABLE**

|  |  |  |
| --- | --- | --- |
| **Input** | | **Output** |
| A | B | Y |
| 0 | 0 |  |
| 0 | 1 |  |
| 1 | 0 |  |
| 1 | 1 |  |

**Methodology**

**Conclusion**

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Lab performed on (date): \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Submitted by: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Registration No.\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Teacher Remarks: \_\_\_\_\_\_\_\_\_\_\_\_\_\_